TEXAS INSTRUMENTS
SN65220, SN65240, SN75240
SLLS266J – FEBRUARY 1997 – REVISED AUGUST 2022

SNx52x0 USB Port Transient Suppressors

1 Features

- Design to protect submicron 3-V or 5-V circuits from noise transients
- Port ESD protection capability exceeds:
  - 15-kV human body model
  - 2-kV machine model
- Available in a WCSP chip-scale package
- Stand-off voltage: 6 V (minimum)
- Low current leakage: 1-µA maximum at 6 V
- Low capacitance: 35-pF (typical)

2 Applications

- USB full-speed host, HUB, or peripheral
- Ports

3 Description

The SN65220 device is a dual, and the SN65240 and SN75240 devices are quadruple, unidirectional transient voltage suppressors (TVS). These devices provide electrical noise transient protection to Universal Serial Bus (USB) low and full-speed ports. The input capacitance of 35 pF makes it unsuitable for high-speed USB 2.0 applications.

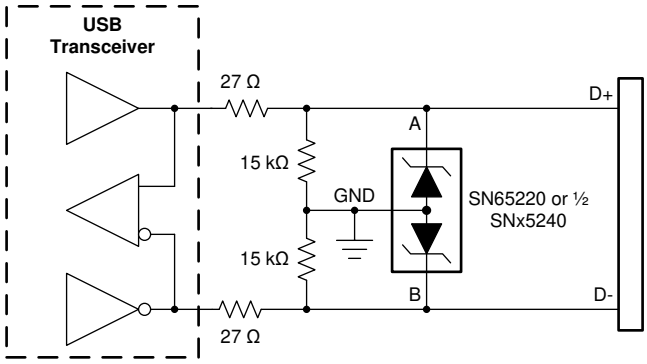
Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the USB transceiver or the USB ASIC if they are of sufficient magnitude and duration.

The SN65220, SN65240, and SN75240 devices ESD performance is measured at the system level, according to IEC61000-4-2; system design, however, impacts the results of these tests. To accomplish a high compliance level, careful board design and layout techniques are required.

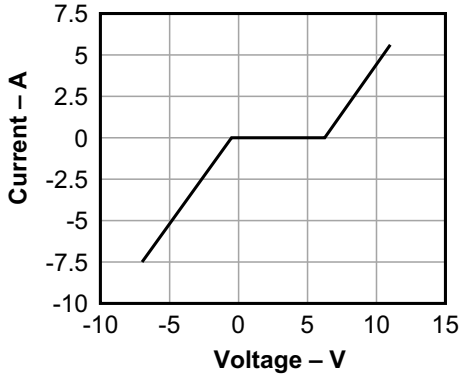
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65220	SOT-23 (6)	2.90 mm × 1.60 mm
	DSBGA (4)	0.925 mm × 0.925 mm
SN65240 SN75240	PDIP (8)	9.09 mm × 6.35 mm
	TSSOP (8)	3.00 mm × 4.40 mm

(1) See the orderable addendum at the end of the data sheet for all available packages.



Simplified Schematic



TVS Current vs Voltage

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (April 2021) to Revision J (August 2022)	Page
• Updated the *SN65220*, *SN65240*, and *SN75240* suppressors in the *Device Comparison* table	3

Changes from Revision H (May 2015) to Revision I (April 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1
• Updated the units for resistance from *O* to *Ω* in the *Simplified Schematic* figure	1
• Updated the units from *O* to *Ω* in the *Typical Application Schematic for ESD Protection of USB Transceivers* figure	8
• Updated the units from *O* to *Ω* in the *Layout Example of a 4-Layer Board With SN65220* figure	10

Changes from Revision G (August 2008) to Revision H (May 2015)	Page
• Added *Pin Configuration and Functions* section, *ESD* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Device Comparison Table

PRODUCT	SUPPRESSORS	T_A - RANGE	PACKAGE
SN65220	2	–40°C to 85°C	WCSP-4
			SOT23-6
SN65240	4	–40°C to 85°C	DIP-8
			TSSOP-8
SN75240	4	0°C to 70°C	DIP-8
			TSSOP-8

6 Pin Configuration and Functions

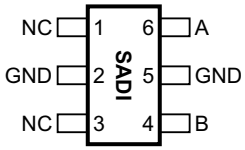


Figure 6-1. DBV Package, 6-Pin SOT-23 (Top View)

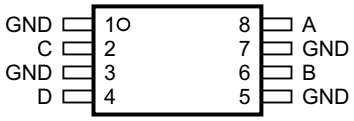


Figure 6-2. P, PW Package,s 8-Pin PDIP, TSSOP (Top View)

Table 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBV	P, PW		
A	6	8	Analog input	Transient suppressor input – Line 1
B	4	6	Analog input	Transient suppressor input – Line 2
C	—	2	Analog input	Transient suppressor input – Line 3
D	—	4	Analog input	Transient suppressor input – Line 4
GND	2, 5	1, 3, 5, 7	Power	Local device ground
NC	1, 3	—	—	Internally not connected

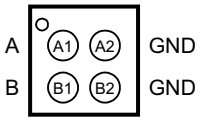


Figure 6-3. YZB Package, 4-Pin DSBGA (Top View)

Table 6-2. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	A	Analog input	Transient suppressor input – Line 1
B1	B	Analog input	Transient suppressor input – Line 2
A2, B2	GND	Power	Local device ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$P_{D(peak)}$	Peak power dissipation		60	W
I_{FSM}	Peak forward surge current		3	A
I_{RSM}	Peak reverse surge current		–9	A
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 7.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±15000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
T_A	Ambient temperature	SN75240	0	70	°C
		SN65220, SN65240	–40	85	

7.4 Thermal Information

THERMAL METRIC(1)		SN65220		SN65240, SN75240		UNIT
		DBV (SOT-23)	YZB (DSBGA)	P (PDIP)	PW (TSSOP)	
		6 PINS	4 BALLS	8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	199.5	170	67.5	185.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	159.7	1.8	57.9	68.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.1	43.5	44.5	114.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	41	9.2	36.2	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.5	43.5	44.5	112.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{lkg}	Leakage current	V_I = 6 V at A, B, C, or D terminals			1	µA
$V_{(BR)}$	Breakdown voltage	V_I = 1 mA at A, B, C, or D terminals	6.5	7	8	V
C_{IN}	Input capacitance to ground	V_I = 0.4 sin (4E6πt) + 0.5 V		35		pF

7.6 Typical Characteristics

T_A = 25°C unless otherwise noted.

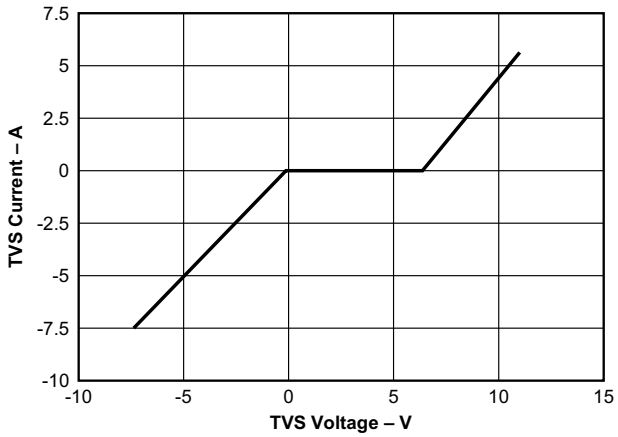


Figure 7-1. Transient-Voltage-Suppressor Current vs Voltage

8 Parameter Measurement Information

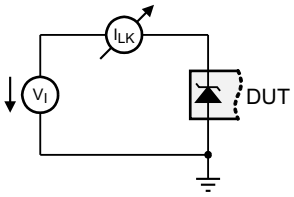


Figure 8-1. Measurement of Leakage Current

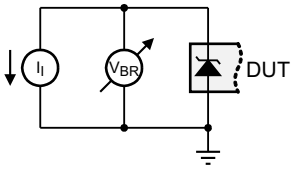


Figure 8-2. Measurement of Breakdown Voltage

9 Detailed Description

9.1 Overview

The SN65220, SN65240, and SN75240 devices integrate multiple unidirectional transient voltage suppressors (TVS). Figure 9-1 shows the equivalent circuit diagram of a single TVS diode.

For positive transient voltages, only the Q1 transistor determines the switching characteristic. When the input voltage reaches the Zener voltage, V_Z, Zener diode D1 conducts; therefore, allowing for the base-emitter voltage, V_{BE}, to increase. At $V_{IN} = V_Z + V_{BE}$, the transistor starts conducting. From then on, its on-resistance decreases linearly with increasing input voltage.

For negative transient voltages, only diode D2 determines the switching characteristic. Here, switching occurs when the input voltage exceeds the diode forward voltage, V_{FW}.

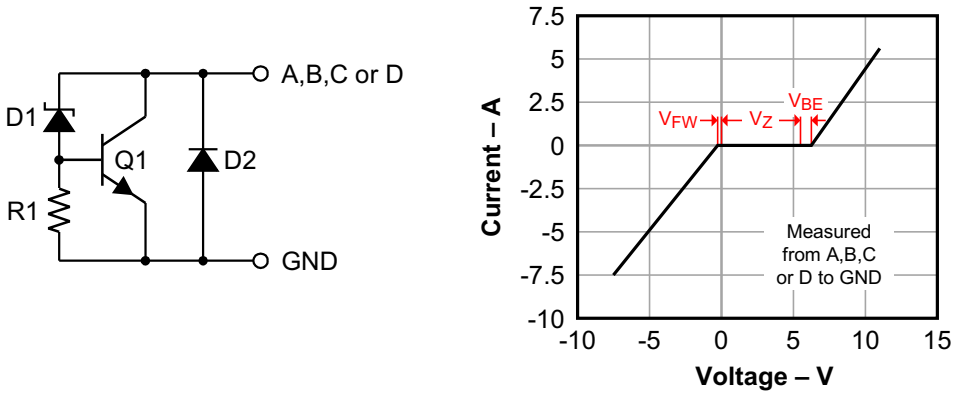
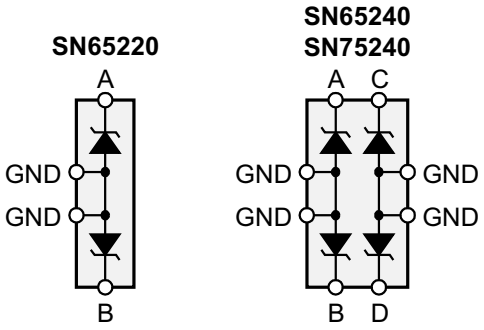


Figure 9-1. TVS Structure and Current — Voltage Characteristic

9.2 Functional Block Diagram



9.3 Feature Description

The SN65220, SN65240, and SN75240 family of unidirectional transient voltage suppressors provide transient protection to Universal Serial Bus low and full−speed ports. These TVS diodes provide a minimum breakdown voltage of 6.5-V to protect USB transceivers and USB ASICs typically implemented in 3-V or 5-V digital CMOS technology.

9.4 Device Functional Modes

TVS diodes possess two functional modes, a high-impedance and a conducting mode.

During normal operating conditions, that is in the absence of high voltage transients, the breakdown voltage of TVS diodes is not exceeded and the devices remain high-impedance.

In the presence of high-voltage transients the breakdown voltage is exceeded. The TVS diodes then conduct and become low-impedance. In this mode excessive transient energy is shunted directly to local circuit ground, preventing USB transceivers from electrical damage.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The USB has become a popular solution to connect PC peripherals. The USB allows devices to be hot-plugged in and out of the existing PC system without rebooting or turning off the PC. Because frequent human interaction with the USB system occurs as a result of its attractive hot-plugging ability, there is the possibility for large ESD strikes and damage to crucial system elements. The ESD protection included on the existing hardware is typically in the 2-kV to 4-kV range for the human body model (HBD) and 200-V to 300-V for the machine model (MM). The ESD voltage levels found in a normal USB operating environment can exceed these levels. The SN75240, SN65240, and SN65220 devices will increase the robustness of the existing USB hardware to ESD strikes common to the environment in which USB is likely to be used.

10.2 Typical Application

Figure 10-1 shows a typical USB system and application of the SN75240, SN65240, and SN65220 devices. Connections to pin A from the D+ data line, pin B from the D– data line, and the device grounds from the GND line that already exists are necessary to increase the amount of ESD protection provided to the USB port.

The design of the suppressor gives it very low maximum current leakage of 1 µA, a very low typical capacitance of 35 pF, and a standoff voltage minimum of 6 V. Because of these levels, the SN75240, SN65240, and SN65220 devices will provide added protection to the USB system hardware during ESD events without introducing the high capacitance and current leakage levels typical of external transient voltage suppressors. The addition of an SN75240, SN65240, or SN65220 device is beneficial to both full-speed and low-speed USB 1.1 bandwidth standards.

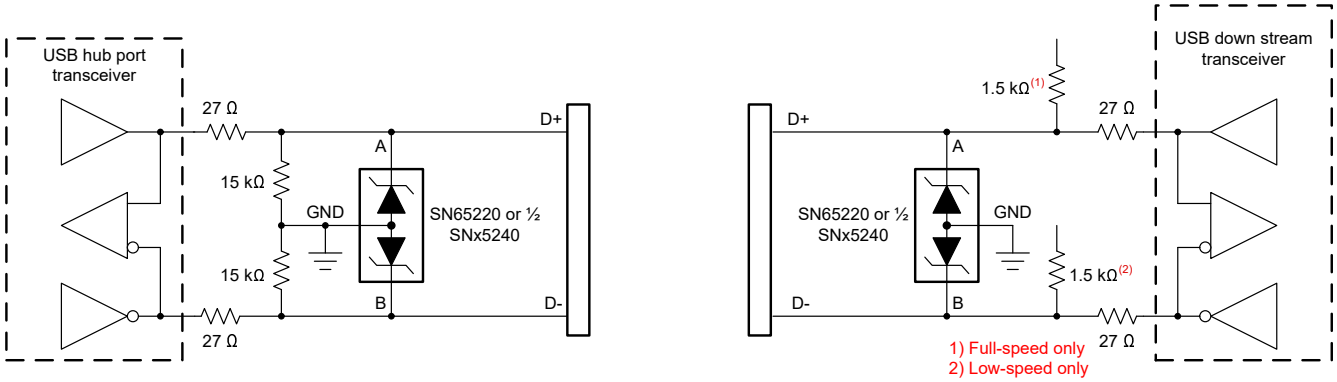


Figure 10-1. Typical Application Schematic for ESD Protection of USB Transceivers

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 10-1 as design parameters.

Table 10-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum breakdown voltage (TVS)	6.5 V
Maximum supply voltage (USB transceiver)	5.5 V
Typical junction capacitance (TVS)	35 pF
Maximum data rate (USB transceiver)	12 Mbps

10.2.2 Detailed Design Procedure

To effectively protect USB transceivers, use TVS diodes with breakdown voltages close to 6 V, such as the SN65220, SN65240, or SN75220 devices.

Because of the TVS junction capacitance of 35 pF, apply these TVS diodes only to USB transceivers with full-speed capability that is 12 Mbps maximum.

Place the TVS diodes as close to the board connector as possible to prevent transient energies from entering further board space.

Connect the TVS diode between the data lines (D+, D–) and local circuit ground (GND).

Because noise transient represents high-speed frequencies, ensure low-inductance return paths for the transient currents by providing a solid ground plane and using two VIAs connecting the TVS terminals to ground.

10.2.3 Application Curve

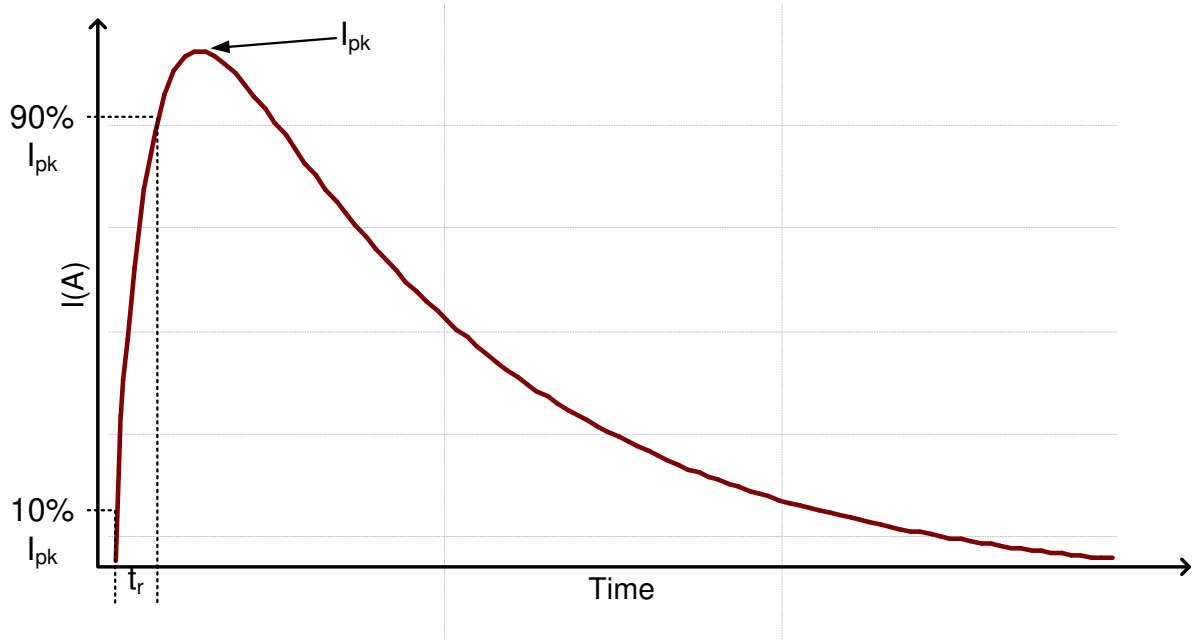


Figure 10-2. HBM Curve

11 Power Supply Recommendations

Unlike other semiconductor components that require a supply voltage to operate, the SN65220, SN65240, and SN75240 transient suppressors are combinations of multiple p-n diodes, activated by transient voltages. Therefore, these transient suppressors do not require external voltage supplies.

12 Layout

12.1 Layout Guidelines

The multiple ground pins provided lower the connection resistance to ground. In order to improve circuit operation, a connection to all ground pins must be provided on the system printed circuit board. Without proper device connection to ground, the speed and protection capability of the device will be degraded.

- The ground termination pads should be connected directly to a ground plane on the board for optimum performance. A single trace ground conductor will not provide an effective path for fast rise-time transient events including ESD due to parasitic inductance.
- Nominal inductive values of a PCB trace are approximately 20 nH/cm. This value may seem small, but an apparent *short length* of trace may be sufficient to produce significant L(di/dt) effects with fast rise-time ESD spikes.
- Mount the TVS as close as possible to the I/O socket to reduce radiation originating from the transient as it is routed to ground.

Note

Direct connective paths of the traces are taken to the suppressor mounting pads to minimize parasitic inductance in the surge-current conductive path, thus minimizing L(di/dt) effects.

12.2 Layout Example

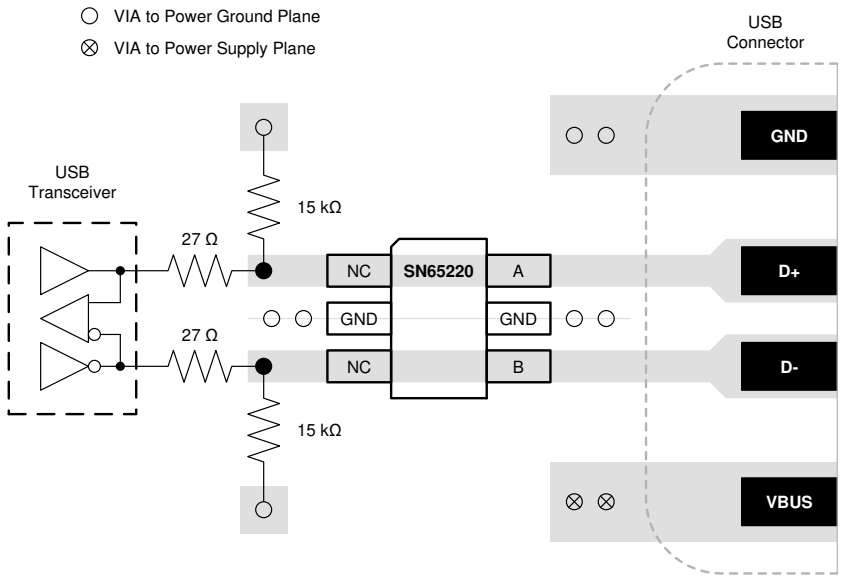


Figure 12-1. Layout Example of a 4-Layer Board With SN65220

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.3 Trademarks

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All trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65220DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SADI
SN65220DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SADI
SN65220DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
SN65220DBVT	Obsolete	Production	SOT-23 (DBV) | 6	-	-	Call TI	Call TI	-40 to 85	SADI
SN65240P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65240P
SN65240P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65240P
SN65240PW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	A65240
SN65240PWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A65240
SN65240PWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A65240
SN75240P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75240P
SN75240P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75240P
SN75240PW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	0 to 70	A75240

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN65220 :

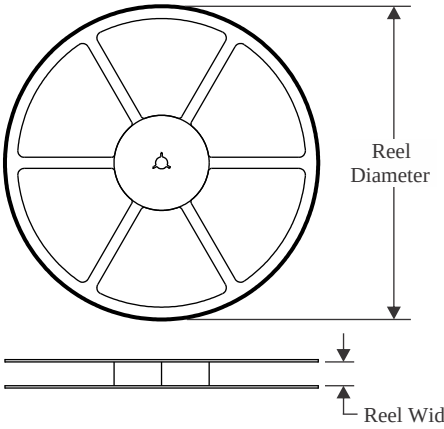
- Automotive : SN65220-Q1

NOTE: Qualified Version Definitions:

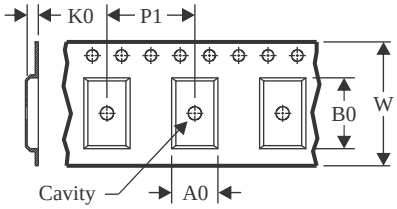
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

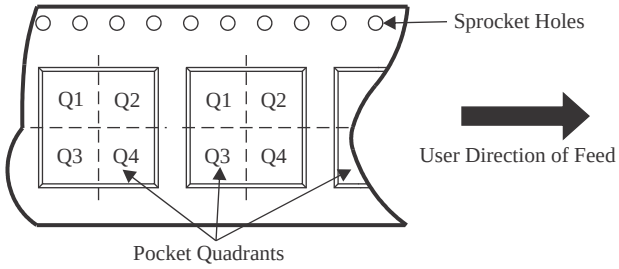


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

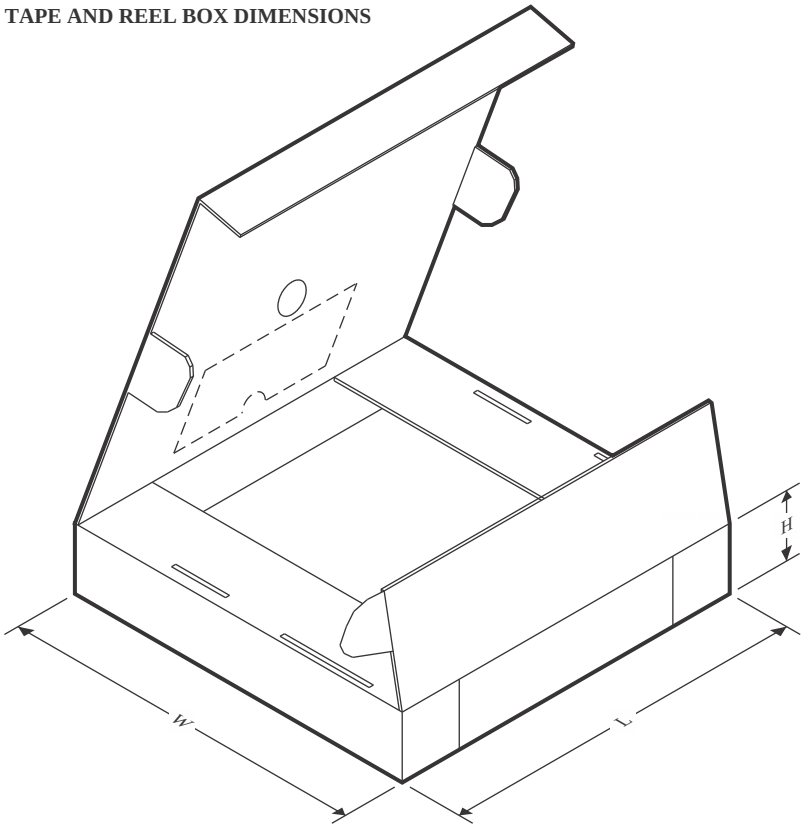
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65220DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN65240PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

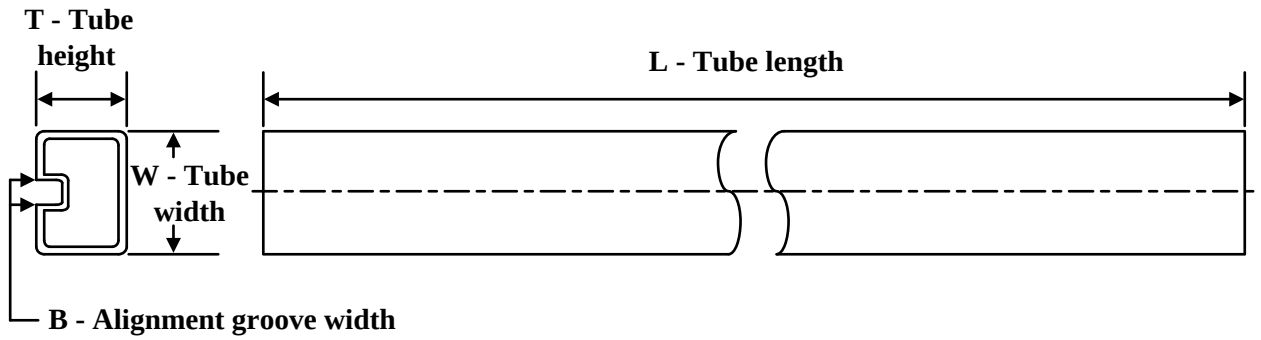
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65220DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN65240PWR	TSSOP	PW	8	2000	356.0	356.0	35.0

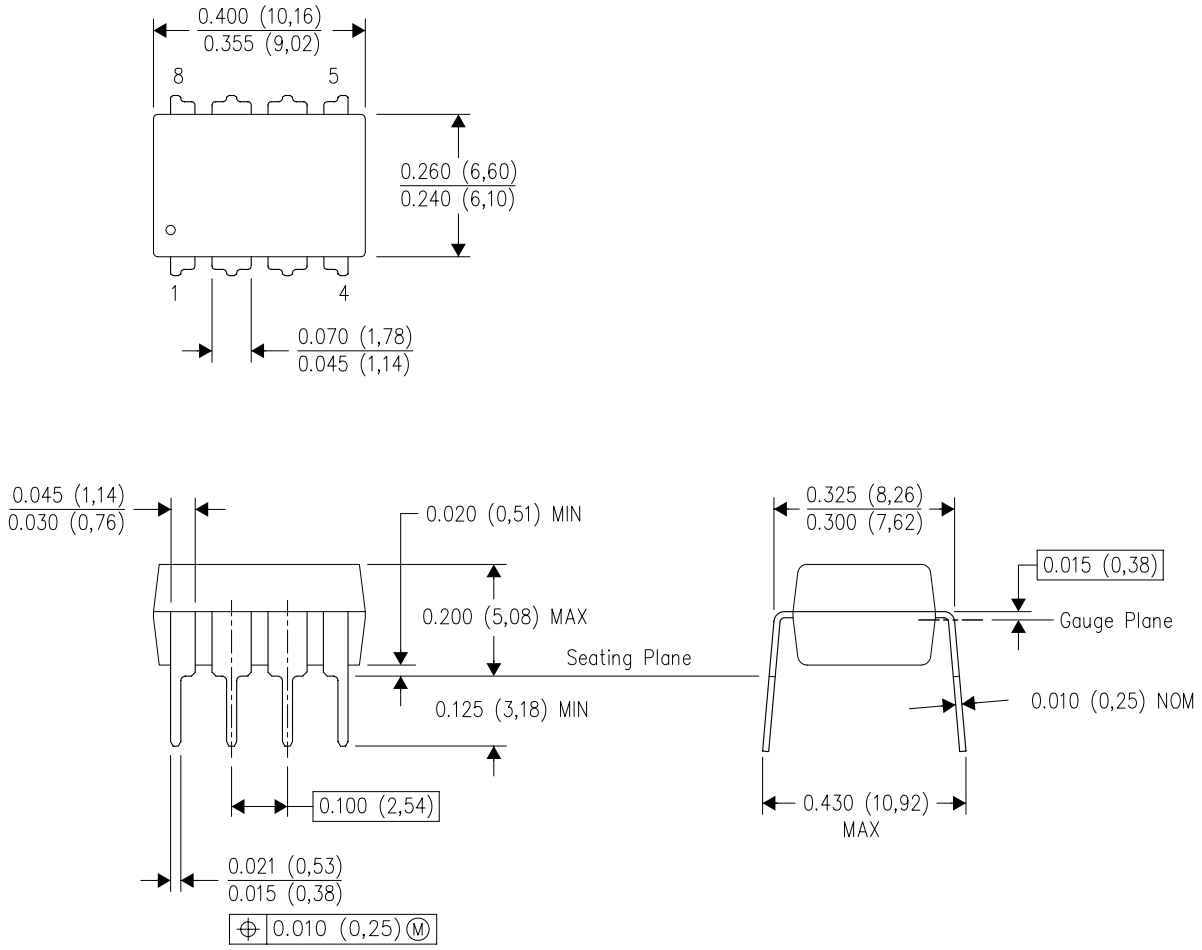
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65240P	P	PDIP	8	50	506	13.97	11230	4.32
SN65240P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75240P	P	PDIP	8	50	506	13.97	11230	4.32
SN75240P.A	P	PDIP	8	50	506	13.97	11230	4.32

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



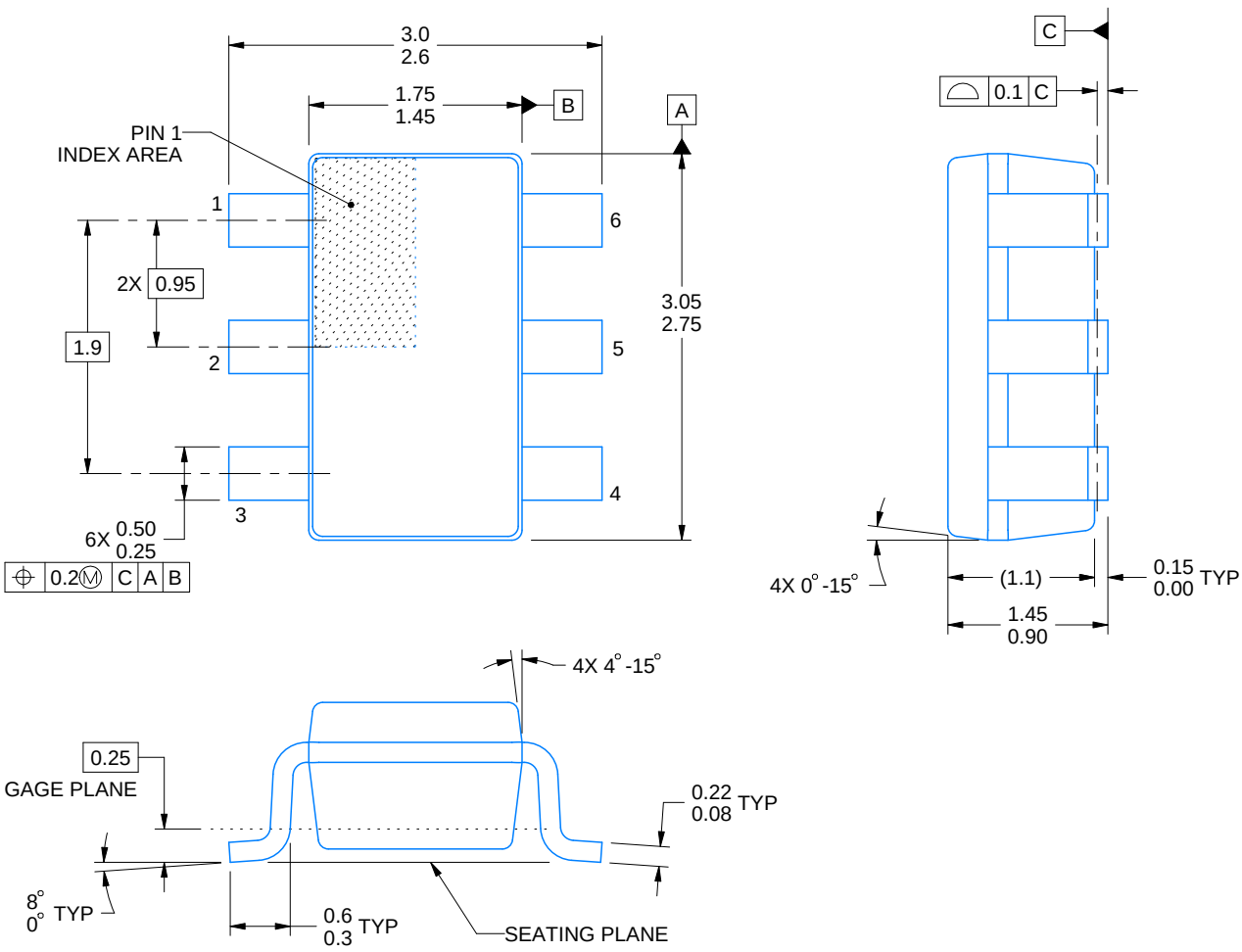
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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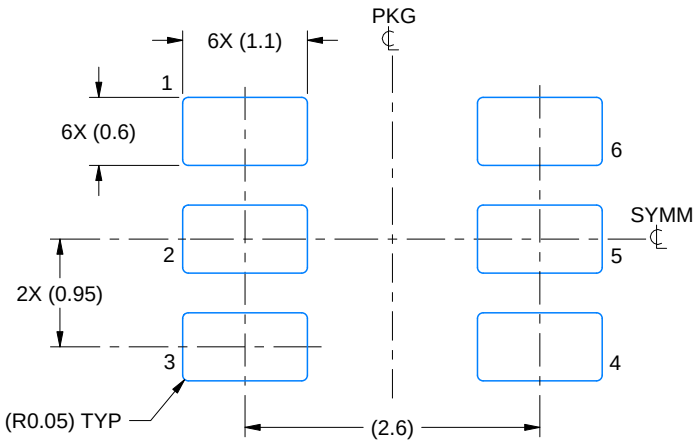
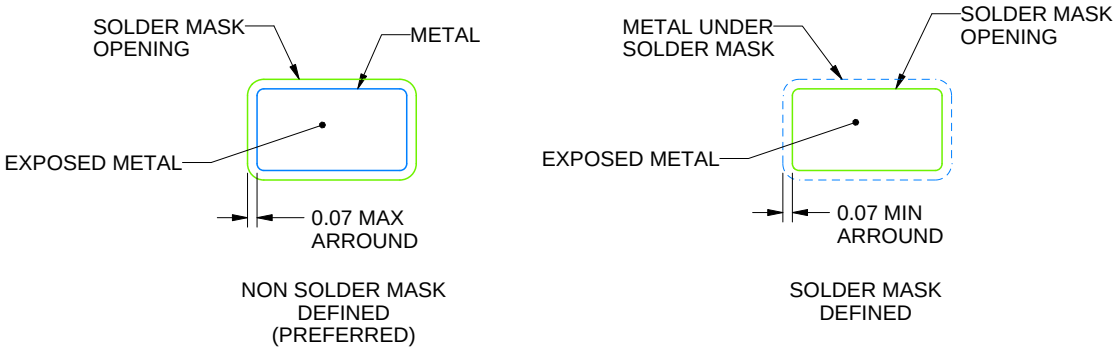
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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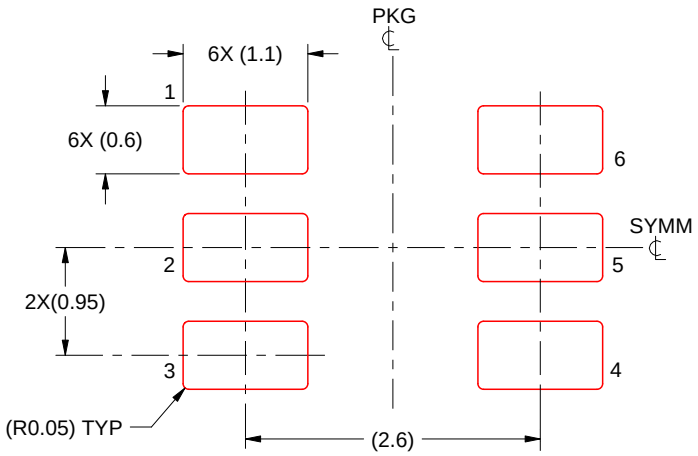
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

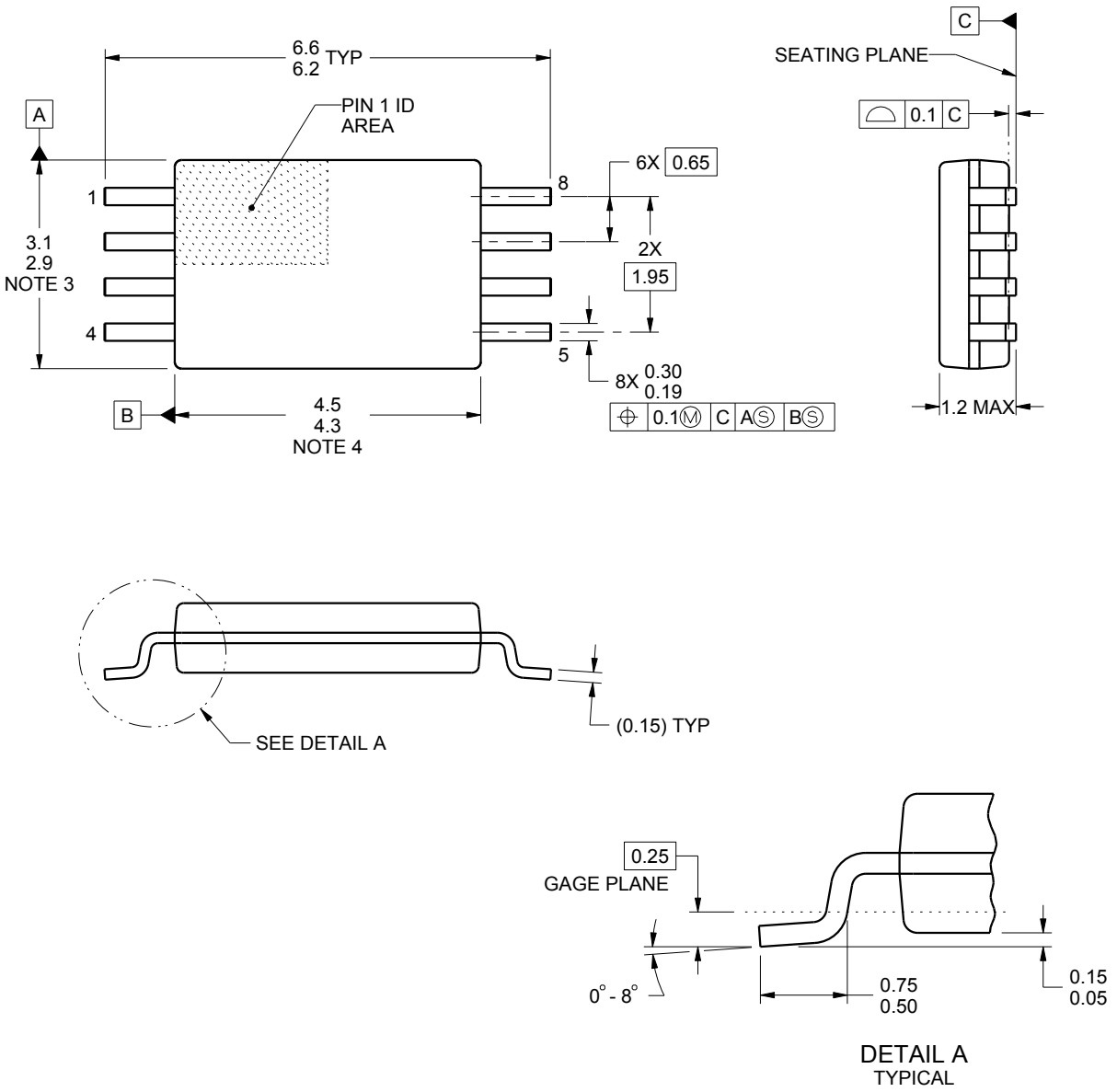
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

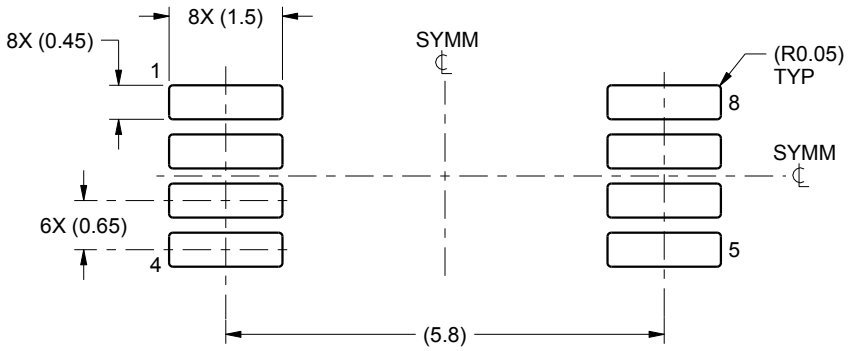
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

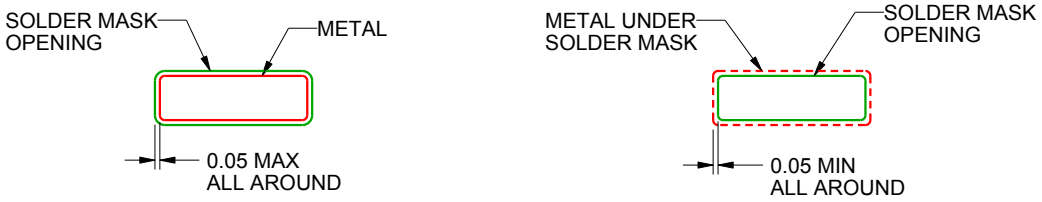


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

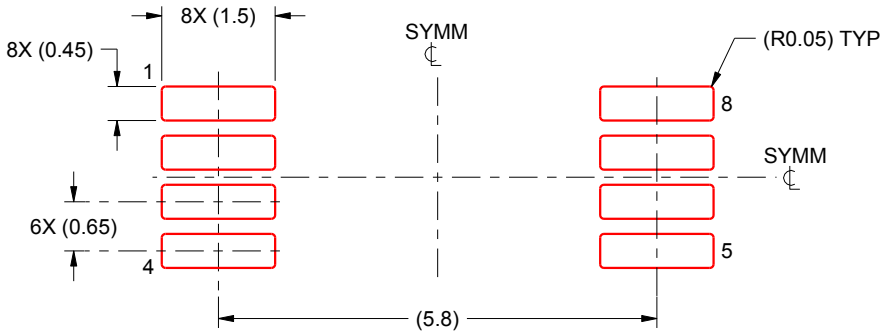


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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